REMARKS

The claims are claims 13 and 25 to 29.

Claim 28 is amended. Claim 28 is amended to include the limitation that the first and second Q shifter operate "responsive to the rounding dot product instruction."

Claim 28 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The FINAL REJECTION states that limitations to the first and second Q shifters are incomplete.

Amended claim 28 is proper under 35 U.S.C. 112. Claim 28 has been amended to explicitly state that the first and second Q shifters operate "responsive to the rounding dot product instruction." The Applicant submits that by this amendment the limitations are complete. Accordingly, claim 28 is proper under 35 U.S.C. 112.

Claims 13 and 25 to 29 were rejected under 35 U.S.C. 101 as directed to non-statutory subject matter. The FINAL REJECTION states that claims 13 and 25 to 29 cite a system and apparatus for performing a dot product in accordance with a mathematical algorithm, merely disclosing steps/components for performing a dot product without further disclosing a practical/physical application or a useful and tangible result. The FINAL REJECTION further states the claims preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein.

Claims 13 and 25 to 29 recite statutory subject matter. Independent claim 13 recites "A digital system." Independent claim

25 recites "A data processing apparatus." Thus the claims in this application are directed to a machine which is of a class of subject matter eligible for patent protection. The application teaches a concrete, useful and tangible application for the data processing apparatus recited in independent claims 13 and 25. This application states at page 2, lines 10 to 17:

> "Special-purpose microprocessors, in contrast, are designed to provide performance improvement for specific predetermined arithmetic and logical functions for which the user intends to use the microprocessor. By knowing the primary function of the microprocessor, the designer can structure the microprocessor architecture in such a manner that the performance of the specific function by the special-purpose microprocessor greatly exceeds the performance of the same function by a general-purpose microprocessor regardless of the program implemented by the user."

Thus this portion of the application states that a special-purpose microprocessor such as disclosed and claimed may implement a specific function with greater performance than a general-purpose microprocessor. This application further state at page 19, lines 3 to 23:

> "In this embodiment, rounding at bit 16 of the 32-bit combined product with a rounding value of 0x8000 (2^{15}) and right shifting sixteen bits is performed in order to reduce processing time required for applications such as IDCT. The inventor of the present invention discovered that source code written for applications such as IDCT in the known C programming language often contains a sequence of instructions such as the following:
>
> "Q1 = (F1*C7 - F7*C1 + 0x8000) >> 16;
> "Q0 = (F5*C3 - F3*C5 + 0x8000) >> 16;
> "S0 = (F5*C5 + F3*C3 + 0x8000) >> 16;
> "S1 = (F1*C1 + F7*C7 + 0x8000) >> 16;
>
> "Advantageously, by using the dot product instructions of the present invention, the C-code sequence above can be directly replaced with a sequence similar to the following, for

example, to reduce instruction count and improve processing performance:

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"Q1    = _dotpnrsu2(F17, C71);
"Q0    = _dotpnrsu2(F53, C35);
"S0    = _dotprsu2 (F53, C53);
"S1    = _dotprsu2 (F17, C17);"
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Thus this application teaches that the invention reduces the number of instructions needed to implement a known C code implementation of an Inverse Discrete Cosine Transform (IDCT) function. As noted in the application at page 2, line 25 to page 3, line 3, the IDCT function is one of a set of problems for with a digital signal processor is suitable for "real-time applications such as image and speech processing." Thus this application teaches a concrete use of an embodiment of the data processing apparatus recited in these claims.

The Applicants submit that the utility asserted in the above quoted portion of the application is substantial and specific. These claims recite a digital system and a data processing apparatus and the asserted utility is a type of data processing which can be preformed by a digital system. The asserted utility employs multipliers MPY 0 and MPY 1, adder 420 and shifter 440 illustrated in Figure 4 in a manner ordinarily expected of such parts by one skilled in the art. Accordingly this asserted utility is more than an insubstantial, nonspecific or throw-away utility.

Claim 13 recites that the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction." Claim 25 similarly recites that the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit" and "operable in response to said dot product instruction to arithmetically combine said first and second products and a '1' input at said mid-position carry input of said predetermined bit

thereby forming a mid-position rounded sum." The Applicant urges that these limitations "breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application." The Applicants urge that these are limitations upon the particular hardware and are particularly adapted to the rounding dot product instruction of this application. Thus this application is to a particular, concrete machine and do not attempt to preempt a mathematical algorithm.

These claims are statutory subject matter because the claimed machine produces a useful, tangible and concrete result. This asserted utility is tied to particular machine limitations. Thus the asserted utility is tangible. The Applicants urge that the use of the claimed machine is repeatable. The claimed machine will provide the same result upon repeated use. Thus this use is concrete. Accordingly, the claims of this application have a practical application with a useful, tangible and concrete result and are thus statutory subject matter.

The above quoted portion of the FINAL REJECTION indicates that the Examiner believes claims 13 and 25 to 29 pre-empts one of the 35 U.S.C. 101 judicial exceptions. Section IV.C.3 of the "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" of the OFFICIAL GAZETTE of November 22, 2005 instruct the Examiner to make a determination whether the claimed invention preempts an abstract idea, law of nature, or natural phenomenon (Sec. 101 judicial exceptions). In particular Section IV.C.3 of the Interim Guidelines state:

> "If an examiner determines that the claimed invention preempts a Sec. 101 judicial exception, the examiner must identify the abstraction, law of nature, or natural phenomenon and explain why the claim covers every substantial practical application thereof."

The Applicants respectfully submit that the FINAL REJECTION

includes only an unsupported statement and fails to make this identification. The Applicants urge that claims 13 and 25 to 29 define a machine and do not attempt to preempt a Sec. 101 judicial exception. The Applicant urges that the rounding dot product operation of this invention could be performed by a properly programmed general-purpose computer. The Examiner has cited the combination of Saishi et al and Pitsianis et al as capable of performing the rounding dot product operation of this invention. Accordingly, grant of a patent on this application would not "cover every substantial practical application of the idea embodied" in claims 13 and 25 to 29. If the Examiner continues to believe that claims 13 and 25 to 29 are non-statutory because they preempt a Sec. 101 judicial exception, the Applicant urges the Examiner to make the identification of the above quoted portion of the Interim Guidelines. In the absence of such a showing, claims 13 and 25 to 29 recite statutory subject matter.

In response to prior arguments that the current claims are apparatus claims and not method claims, the FINAL REJECTION states at page 10, lines 4 to 6:

> "The examiner respectfully submits that the claims are still directed to non-statutory subject matter under current language. The claims only disclose the general circuit components for performing basic mathematical operations."

The Applicant respectfully urges that this is incorrect. A claim to a machine would be statutory subject matter even if its only practical use were in performing a mathematical operation. An assembly of general circuit components can be arranged and connected in a novel, unobvious manner. Such an assembly would be statutory subject matter. The Applicant urges that the recited "general circuit components" in claims 13 and 25 to 29 are so arranged and connected as to constitute statutory subject matter.

Claim 13 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al U.S. Patent No. 6,167,419 and Pitsianis et al. U.S. Patent Application Publication No. 2003/00088601.

Claim 13 recites subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 13 recites "an adder/subtractor circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers." The FINAL REJECTION cites elements 506 to 508 illustrated in Figure 5 of Saishi et al as making obvious the claimed adder/subtractor circuit, rounding signal 515 as making obvious the input to the claimed mid-position carry input of the adder/subtractor circuit. The Applicant respectfully submits that these elements of Saishi et al do not make obvious the claimed adder/subtractor circuit because Saishi et al teaches rounding at a different place than recited in claim 13. Saishi et al states at column 12, lines 16 to 23:

> "numeral 506 designates a first subproduct addition means as a component of the multiplication means 503, numeral 507 designates an intermediate register for temporarily storing an intermediate result from the first subproduct addition means 506, numeral 508 designates a second subproduct addition means for adding the output of the intermediate register 507 and used as a component of the multiplication means 503, numeral 509 designates a multiplication result obtained after rounding and used as the output of the second subproduct addition means 508"

Thus Saishi et al clearly states that elements 506 to 508 do not form an adder/subtractor circuit but are part of the multiplication means 503. This portion of Saishi et al teaches that multiplication means 503 produced a product output at element 509. Claim 13 recites that the adder/subtractor circuit receives product output at its inputs. These product outputs correspond to element

509 taught in Figure 5 of Saishi et al. However, Saishi et al teaches no supply of this product 509 to an adder/subtractor circuit. Saishi et al teaches supply of product 509 to switching means 520 and then to barrel shifter 510 and shift and multiplication results register 511. Thus Saishi et al teaches rounding during subproduct addition within a single multiplication rather than while adding or subtracting plural products as recited in claim 13. Combining the teaching of Pitsianis et al with the teaching of Saishi et al would result in plural multipliers each rounding as taught in Saishi et al and adding the rounded products as taught in Pitsianis et al, perhaps eliminating the rounding following the addition taught in Pitsianis et al. Accordingly, claim 13 is allowable over the combination of Saishi et al and Pitsianis et al.

Rounding in the adder/subtractor circuit of claim 13 is unobvious over the combination of Saishi et al and Pitsianis et al. Pitsianis et al teaches production of two products but does not teach a single adder/subtractor circuit combining two products and rounding. Figure 6 of Pitsianis et al teaches combining products in subtractor 623 and adder 625, and rounding the selection and rounder circuit 627. Figure 7 of Pitsianis et al teaches combining products in adder 723 and subtractor 725, and rounding in selection and rounder circuit 727. Figure 17 of Pitsianis et al teaches combining products in adder block 1723 and adder block 1725, and rounding in selection and rounder circuit 1727. Figure 18 of Pitsianis et al teaches combining products in adder block 1823 and adder block 1825, and rounding in selection and rounder circuit 1827. The Applicants respectfully submit that both Saishi et al and Pitsianis et al teach rounding in a portion of the circuit different from that recited in claim 13. As noted above, Saishi et al teaching rounding as part of subproduct addition within a single multiplication resulting in a rounded product. Pitsianis et al

teaches a separate circuit or operation applied after combining the products. In contrast, claim 13 recites both combining the products and rounding in the claimed adder/subtractor circuit. Accordingly, claim 13 is not made obvious by the combination of Saishi et al and Pitsianis et al.

Claims 13 recites further subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 13 recites the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction." The innovation of this application is combining operations normally requiring two hardware circuits into a single hardware circuit. The two combined operations are the sum/difference of the two products and rounding the result. Those skilled in the art would understand the claimed adder/subtractor circuit to include a chain of plural bit circuits. Each bit circuit receives a carry input from the immediately prior bit circuit and supplies a carry output to the immediately following bit circuit. As recited in claim 13, rounding results when an active carry signal is supplied to the mid-position carry input of this bit circuit chain. Even if first subproduct addition means 506 of Saishi et al is regarded as the claimed adder/subtractor circuit, Saishi et al fails to teach this use of a mid-position carry input to a predetermined bit for the recited rounding. Saishi et al states at column 8, lines 27 to 35:

> "When the range indicated by the bit range 804 of the multiplication result 803 is desired to be cut out, and when it is assumed that the predetermined rounding position 811 is basically located at the mth bit from the least significant bit in consideration of the fact that a shift count required for a shift operation for cutting out is indicated by a right shift 809 of kbits, a signal having '1' at the (m+k)th bit is generated as the rounding signal. In other words, the rounding position is shifted to the left by k bits."

This clearly teaches that the rounding position is selected by the rounding generator generating a rounding signal shifted to correspond to the later shift of the rounded product. One skilled in the art would understand the recited "shifted to the left by k bits" to be a multibit signal having 0's shifted into the k least significant bits to place a single 1 bit in the desired rounding position. Figures 1 to 5 of Saishi et al show this rounding signal applied to a normal data input of an addition means. Saishi et al never states that the rounding signal is input to "a mid-position carry input to a predetermined bit" as recited in claim 13. The FINAL REJECTION fails to cite any portion of Saishi et al as making obvious the recited mid-position carry input to a predetermined bit. One skilled in the art would understand Saishi et al to teach supply of a multi-bit rounding signal to an ordinary multi-bit data input of the adder. The left shifted 1 generated by the rounding signal generator is thus supplied to a data input and not to the carry input of a predetermined bit recited in claim 13. Thus Saishi et al teaches achieving the same result of this invention using a different method step or different apparatus. While the FINAL REJECTION states that this is disclosed in Saishi et al, in fact neither addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406, nor first subproduct addition means 506 illustrate the "mid-position carry input to a predetermined bit" recited in claim 13. The description of these parts in Saishi et al indicates that the rounding signal is supplied to a data input of the corresponding addition means. Saishi et al states at column 6, lines 11 to 14:

> "The multiplication result 104 and the rounding signal 106 are input to the addition means 109, and the addition means 109 outputs the multiplication result 110 obtained after rounding."

Saishi et al states at column 10, lines 50 to 53:

> "The subproducts 305 and the rounding signal 315 are added by the first subproduct addition means 306."

This disclosure with the teaching of Saishi et al that the rounding signal is "shifted to the left by k bits" makes clear that the rounding signal is supplied to each bit of a multi-bit input of addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406 and first subproduct addition means 506 rather than the "mid-position carry input to a predetermined bit" recited in claim 13. The FINAL REJECTION does not allege that Pitsianis et al makes obvious this subject matter. Accordingly, claim 13 is not made obvious by the combination of Saishi et al and Pitsianis et al.

Claims 25 to 27 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al U.S. Patent No. 6,167,419 and Peleg et al U.S. Patent No. 6,385,634.

Claim 25 recites subject matter not made obvious by the combination of Saishi et al and Peleg et al. The rejection of claim 25 is essentially the same as the rejection of claim 13. The FINAL REJECTION cites essentially the same portions of Saishi et al and subject matter of Peleg et al similar to the cited portions of Pitsianis et al in the rejection of claim 13. Claim 25 is similarly unobvious over the combination of Saishi et al and Peleg et al. The portions of Saishi et al cited as making obvious the adder/subtractor circuit recited in claim 25 are taught as part of multiplication means 503. Since claim 25 recites the adder/subtractor circuit receives a product output, this limitation is not made obvious by Saishi et al. Claim 25 recites that the combination of the products and rounding take place in the adder/subtractor circuit. Saishi et al teaches rounding taking

place in multiplication means 503. The FINAL REJECTION does not allege that Peleg et al teaches rounding. Claim 25 recites the adder/subtractor circuit includes "a mid-position carry input to a predetermined bit" and is operable "to arithmetically combine said first and second products and a '1' input at said mid-position carry input of said predetermined bit thereby forming a mid-position rounded sum." The Applicant respectfully urges that the combination of Saishi et al and Peleg et al fail to make obvious such a mid-position carry input. Accordingly, claim 25 is allowable over the combination of Saishi et al and Peleg et al.

Claims 26 and 27 are allowable by dependence upon allowable claim 25.

Since there is no art rejection of claims 28 or 29 and these claims are statutory subject matter, claims 28 and 29 are allowable.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. The amendment to claim 28 includes the limitation that the Examiner assumed for examination purposes. Thus no new search or consideration is required by this amendment.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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